IN THE CLAIMS:

Please amend Claims 1, 3, and 6 as shown in this complete set of all pending Claims:

1. (Currently amended) A protection circuit associated with a first PMOS transistor of a voltage specification of a first voltage level, said first PMOS transistor and said protection circuit being comprised in an integrated circuit designed to process information in an input signal having a swing equaling a second voltage level, wherein said first voltage level is lower than said second voltage level, said protection circuit comprising:

a second PMOS transistor which switches to an off state if said input signal having said swing would cause a cross terminal voltage of said first PMOS transistor to exceed a permissible range, wherein said second PMOS transistor in said off state ensures that said cross terminal voltage of said first PMOS transistor does not exceed said permissible range;

a first NMOS transistor also of said voltage specification of said first voltage level;

a second NMOS transistor which switches to an off state if said input signal would cause a cross terminal voltage of said first NMOS transistor to exceed a permissible range, wherein said second NMOS transistor in said off state ensures that said cross terminal voltage of said first NMOS transistor does not exceed said permissible range.

2. (Canceled)

3. (Currently amended) The protection circuit of claim [[2]] 1, wherein a source terminal of said first PMOS transistor being connected to a supply voltage of said second voltage level.

4. (Original) The protection circuit of claim 3, wherein said input signal swings between a reference voltage and said second voltage level.

5. (Canceled)

6. (Currently amended) The protection circuit of claim [[5]] 1, wherein an upper limit of said permissible range equals an allowed maximum voltage associated with each of said first PMOS transistor and said first NMOS transistor.

11. (Original) The protection circuit of claim 6, said protection circuit further comprising:

a third NMOS transistor, a gate terminal of said third NMOS transistor being connected to said second bias voltage, a source terminal of said third NMOS transistor being connected to a gate terminal of said first NMOS transistor,

a drain terminal of said first NMOStransistor being connected to a source terminal of said second NMOS transistor, and a source terminal of said first NMOStransistor being connected to a reference voltage,

wherein said third NMOS transistor ensures that a gate to source voltage (Vgs) and a gate to drain voltage (Vgd) of said first NMOStransistor from being exposed to voltage exceeding said permissible range.

12. (Original) The protection circuit of claim 11, wherein said input buffer further comprises a fourth NMOS transistor, a gate terminal of said fourth NMOS transistor being connected to said source terminal of said second NMOS transistor, a drain terminal of said fourth NMOS transistor connected to said source terminal of said third NMOS transistor, and a source terminal of said fourth NMOS transistor being connected to said reference voltage.

13. (Original) The protection circuit of claim 12, wherein all of said first NMOS transistor, said second NMOS transistor, said third NMOS transistor, and said fourth NMOS transistor are of said voltage specification of said first voltage level.